

WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device,  
comprising:

forming a protective layer over a polysilicon gate electrode  
located over a substrate to provide a capped polysilicon gate  
electrode;

forming source/drain regions in said substrate proximate said  
capped polysilicon gate electrode;

removing said protective layer using an etchant;

siliciding said polysilicon gate electrode to form a silicided  
gate electrode; and

siliciding said source/drain regions.

2. The method as recited in Claim 1 further including  
forming a silicide blocking layer over said source/drain regions  
prior to said siliciding said polysilicon gate electrode.

3. The method as recited in Claim 2 wherein forming a  
silicide blocking layer includes growing a silicide blocking layer  
using a dry oxidation process.

4. The method as recited in Claim 2 wherein forming a  
silicide blocking layer includes growing a silicide blocking layer

3 using a low temperature radical oxidation or plasma oxidation  
4 process.

5. The method as recited in Claim 2 wherein forming a  
2 silicide blocking layer includes forming a silicide blocking layer  
3 having a thickness ranging from about 2 nm to about 10 nm.

6. The method as recited in Claim 1 wherein said protective  
2 layer is a silicon nitride protective layer.

7. The method as recited in Claim 6 further including  
2 forming a sidewall spacer adjacent said capped polysilicon gate  
3 electrode that includes a nitride layer wherein said nitride layer  
4 is of a different chemical composition than said silicon nitride  
5 protective layer.

8. The method as recited in Claim 7 wherein said nitride  
2 layer has from about 5% to about 10% carbon content.

9. The method as recited in Claim 1 wherein said silicided  
2 source/drain regions extend under at least a portion of gate  
3 sidewall spacers located adjacent said silicided gate electrode.

10. The method as recited in Claim 1 wherein the protective  
2 layer has a thickness ranging from about 5 nm to about 50 nm.

11. A semiconductor device, comprising:

2 a silicided gate electrode located over a substrate, said  
3 silicided gate electrode having gate sidewall spacers located on  
4 sidewalls thereof;

5 source/drain regions located in said substrate proximate said  
6 silicided gate electrode; and

7 silicided source/drain regions located in said source/drain  
8 regions and at least partially under said gate sidewall spacers.

12. The semiconductor device as recited in Claim 11 wherein  
2 said silicided source/drain regions extend from about 2 nm to about  
3 10 nm under said gate sidewall spacers.

13. The semiconductor device as recited in Claim 11 wherein  
2 said silicided source/drain regions have a thickness ranging from  
3 about 10 nm to about 30 nm.

14. A method for manufacturing an integrated circuit,  
comprising:

forming semiconductor devices over a substrate, including;  
forming a protective layer over a polysilicon gate  
electrode located over said substrate to provide a capped  
polysilicon gate electrode;

forming source/drain regions in said substrate proximate  
said capped polysilicon gate electrode;

removing said protective layer using an etchant;

siliciding said polysilicon gate electrode to form a  
silicided gate electrode; and

siliciding said source/drain regions; and

forming interconnects within dielectric layers located over  
said substrate for electrically contacting said semiconductor  
devices.

15. The method as recited in Claim 14 further including  
forming a silicide blocking layer over said source/drain regions  
prior to said siliciding said polysilicon gate electrode.

16. The method as recited in Claim 15 wherein forming a  
silicide blocking layer includes growing a silicide blocking layer  
using a dry oxidation process.

17. The method as recited in Claim 15 wherein forming a silicide blocking layer includes growing a silicide blocking layer using a low temperature radical oxidation or plasma oxidation process.

18. The method as recited in Claim 15 wherein forming a silicide blocking layer includes forming a silicide blocking layer having a thickness ranging from about 2 nm to about 10 nm.

19. The method as recited in Claim 14 wherein said protective layer is a silicon nitride protective layer.

20. The method as recited in Claim 19 further including forming a sidewall spacer adjacent said capped polysilicon gate electrode that includes a nitride layer wherein said nitride layer is of a different chemical composition than said silicon nitride protective layer.

21. The method as recited in Claim 20 wherein said nitride layer has from about 5% to about 10% carbon content.

22. The method as recited in Claim 14 wherein said silicided source/drain regions extend under at least a portion of gate sidewall spacers located adjacent said polysilicon gate electrode.

23. The method as recited in Claim 14 wherein the protective  
2 layer has a thickness ranging from about 5 nm to about 50 nm.